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(54) **High-frequency circuit comprising an integrated capacitor**

(57) A high-frequency circuit (11) having at least a semiconductor circuit element (12) which is arranged on the side of a first surface (13) of an insulating substrate (14). At least one (19a, 19b) of the output terminals (17, 18a, 18b, 19a, 19b) of the semiconductor circuit element (12) is intended to be electrically connected to a ground plane (16) through a capacitive element (20) and metallized holes (21, 22). According to the invention, the circuit element (12) is secured on a plate (24) of a dielectric material provided with conducting "bumps" (27, 28a, 28b, 29a, 29b) on which the said output terminals are soldered, the "bumps" on which the terminals (19a, 19b) are secured being conductively connected to metallized surfaces (30a, 30b) constituting a first plate of the capacitive element (20), while a conducting surface (31) formed between the plate (24) and the substrate (14) constitutes a second plate of the said capacitive element.

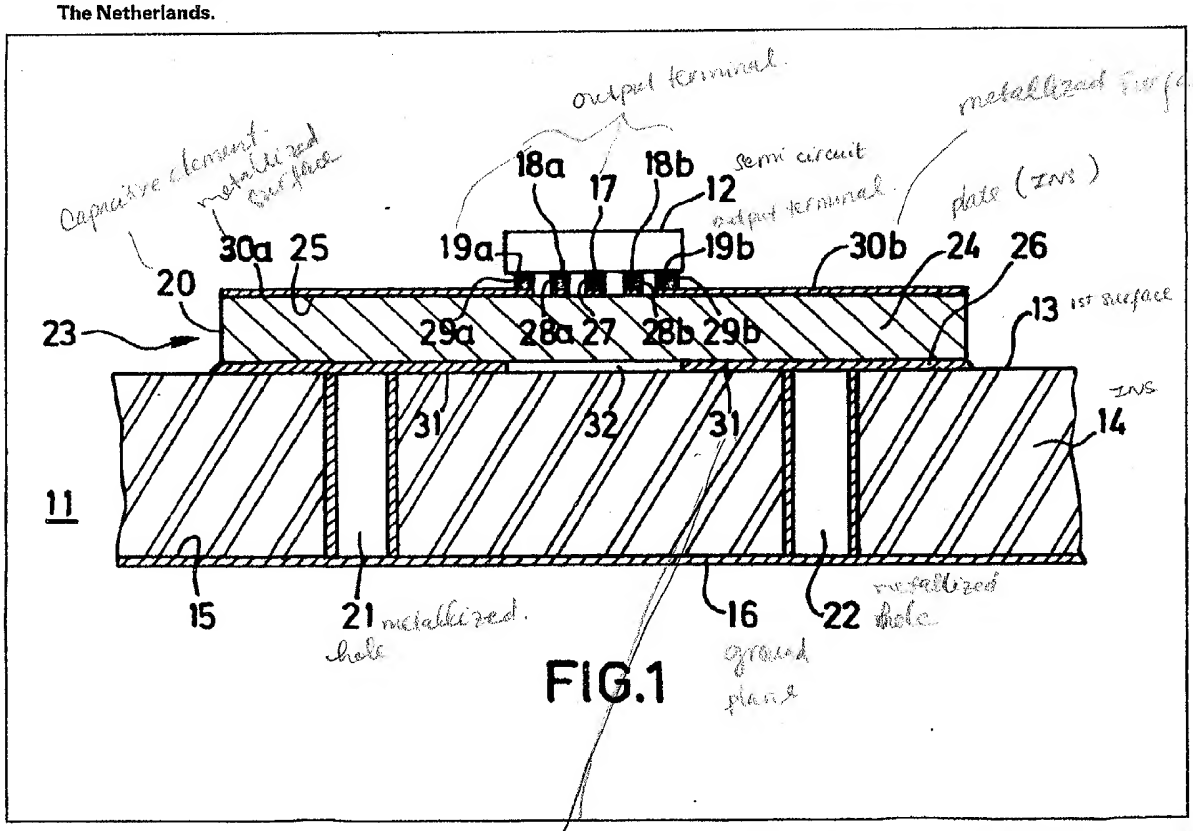

FIG.1

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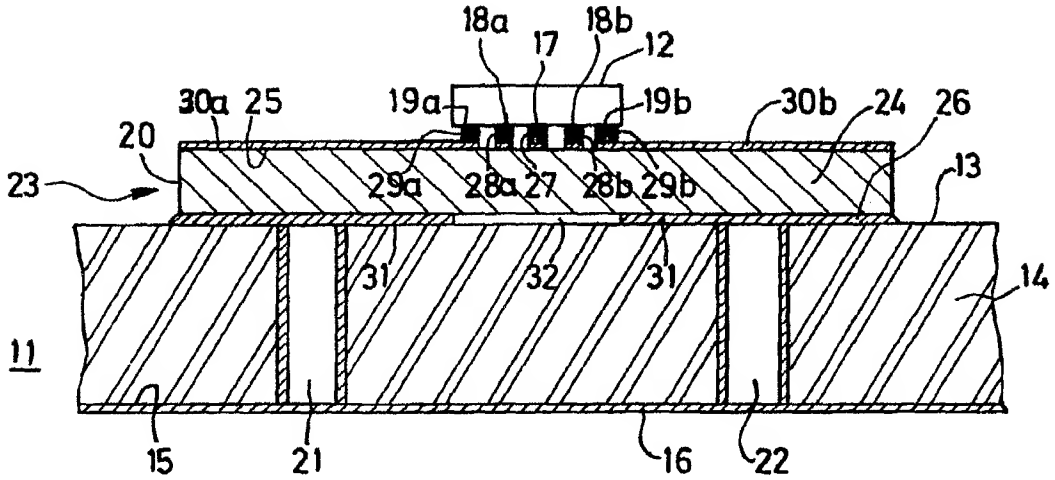

FIG.1

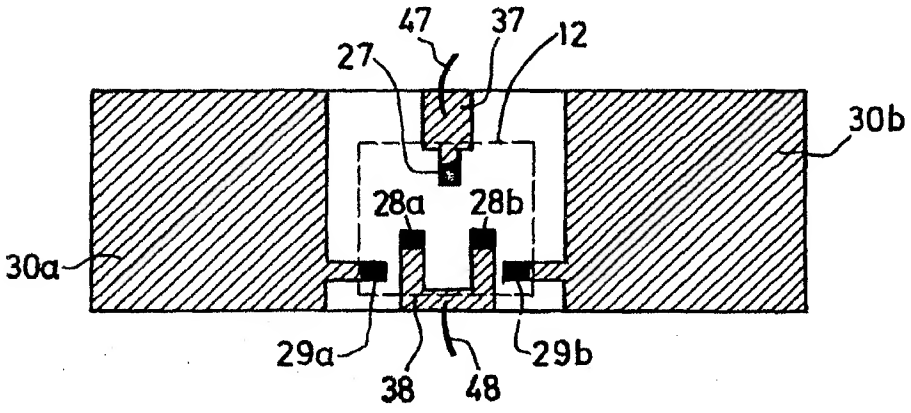

FIG.2

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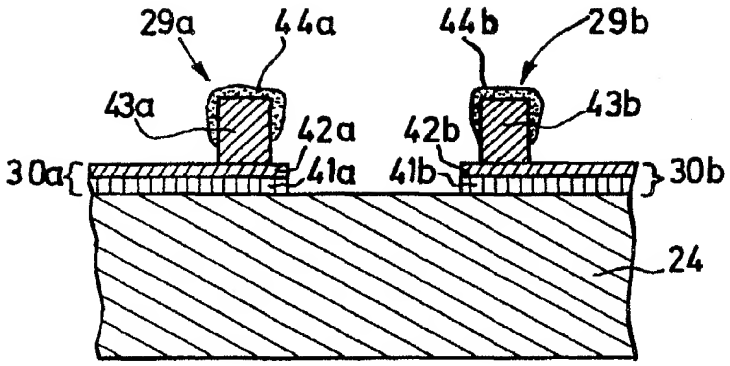

FIG.3

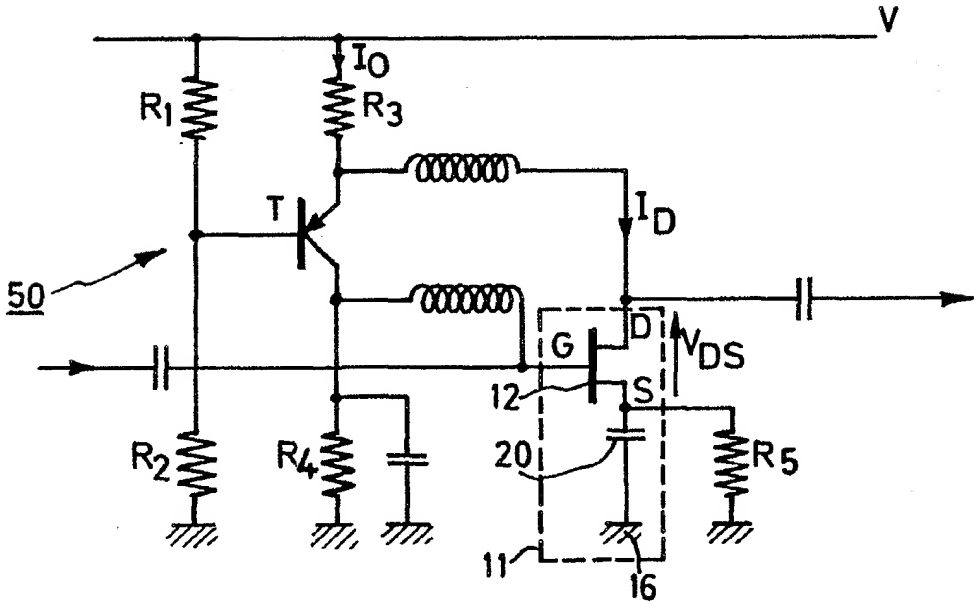

FIG.4

SPECIFICATION

High-frequency circuit comprising an integrated capacitor

The invention relates to a high-frequency circuit comprising at least a semiconductor circuit element which is arranged on the side of a first surface of an insulating substrate, a second surface of this substrate located opposite to the first surface being at least partly metallized in order to form a ground plane, while the semiconductor circuit element is provided with electrodes each having at least an output terminal, one of the electrodes, which is referred to as first electrode, being intended to be electrically connected to the ground plane through a capacitive element and an electrical connection with the ground plane being established by means of a metallized hole through the insulating substrate.

The invention is suitable for use in the field of circuits which operate in the high-frequency range and more particularly circuits comprising field effect transistors.

In the circuits known hitherto of the type described in the preamble, the semiconductor circuit element is generally arranged directly on the conducting surface which is formed on the first surface of the insulating substrate. The output terminals of the electrodes of the semiconductor circuit element are then connected through wires to the other circuit elements of the circuit; this is more particularly the case with the electrical connection between the first electrode and the capacitive element. Now providing the wiring is an operation which has to be effected with great care and which, especially when a large number of output terminals is present, is time-consuming and hence expensive. On the other hand, with this known technology, a good reproducibility of the electrical connections is not always obtained.

The present invention has for its object to obviate this disadvantage by avoiding to the greatest possible extent the use of wiring at the level of the output terminals of the semiconductor circuit element.

According to the invention, such a high-frequency circuit is characterized in that the semiconductor circuit element is secured on an intermediate connection element provided with a plate of a dielectric material having protruding parts of a conducting material which are present on a first surface and on which the output terminals of the electrodes of the semiconductor circuit element are directly soldered, each protruding part, which is connected to output terminals of the first electrode, being conductively connected to a conducting surface which is formed on the first surface of the plate and constitutes a first plate of the capacitive element, while a second surface of the plate, which is located opposite to the first surface, is secured on at least one first surface of the insulating substrate formed on the conducting surface, which contacts at least one metallized hole and constitutes the second plate of the capacitive element. In this way by direct securing of the semiconductor circuit element by means of soldering the output terminals to the protruding parts of the intermediate connection element, interconnection by means of wiring is prevented.

On the other hand, the invention provides the possibility of a simpler manipulation of the semiconductor circuit element so that it can be arranged on an intermediate connection element whose dimensions can be considerably larger than those of the circuit element itself; consequently, the circuit element can be tested more readily before the connection element is secured on the insulating substrate. Finally, the invention further provides the possibility of completely integrating the capacitive element, the intermediate element then serving at the same time as dielectric for the capacitive element.

In a favourable embodiment of the invention, the semiconductor circuit element is a field effect transistor and the said first electrode contacts the source zone of the field effect transistor. In fact, when the use of wires for the connection between the source zone and the ground plane is avoided, the impedance, which is always unfavourable and which is introduced by the said wires, can be eliminated. In a number of applications, it may be of importance that the capacitive element has a high capacitance; the dielectric material of the intermediate wiring board the preferably has a dielectric constant between 600 and 2000.

In order to reduce the capacitance of the conductors, a recess is provided in the conducting surface opposite to the semiconductor element.

When the semiconductor circuit element is a field effect transistor, due to the possibility of connecting the source zone to the ground plane through a capacitive element of high capacitance, a high-frequency circuit can be provided according to the invention characterized in that the source zone of the field effect transistor is capacitively connected for the high frequencies to earth through the said intermediate element and a resistor of fixed value arranged parallel to the capacitive element connects the source zone for low frequencies to earth, while the current and the voltage of the field effect transistor are adjusted through a stabilization circuit so that the working point is independent of the field effect transistor.

The invention will now be described more fully with reference to the accompanying drawings, in which;

Figure 1 is a sectional view of a high-frequency circuit according to the invention,

Figure 2 is a plan view of the intermediate element of a circuit according to the invention,

Figure 3 is a sectional view of an embodiment of the metallized surface and of the metal "bumps" deposited on the first surface of the intermediate element,

Figure 4 shows the circuit diagram of an embodiment of a high-frequency circuit according to the invention, in which a field effect transistor is used.

Figure 1 is a sectional view of a high-frequency circuit 11 provided with a semiconductor circuit element 12, which in the embodiment of Figure 1 is a field effect transistor made, for example, of gallium arsenide. This transistor 12 is arranged on the side of a first surface 13 of an insulating substrate 14 of, for example, aluminium oxide. A second surface 15 of

this substrate, which is located opposite to the first surface 13, is metallized at least in part in order to form a ground plane 16. The field effect transistor 12 is provided with electrodes which contact the drain, the gate and the source zones and are provided with output terminals 17, 18a, 18b, 19a, 19b. In the embodiment shown in Figure 1, the terminal 17 contacts the drain of the transistor, while the terminals 18a and 18b contact the gate and the terminals 19a and 19b contact the source zone. One of the electrodes of the transistor, in the case of Figure 1 that of the source zone, is intended to be electrically connected to the ground plane 16 through a capacitive element 20, the connection to the ground plane 16 being partly realized through two metallized holes 21, 22 through the insulating substrate 14. As can be seen in Figure 1, the field effect transistor 12 is secured on an intermediate element which consists of a plane 24 of a dielectric material provided at one surface 25 with conducting "bumps" 27, 28a, 28b, 29a, 29b, on which the output terminals 17, 18a, 18b, 19a and 19b of the electrodes of the field effect transistor are directly soldered. Each "bump" 29a and 29b corresponding to each of the output terminals 19a and 19b of the source zone is conductively connected to a metallized surface 30a, 30b deposited on the first surface 25 of the plate 24 and constitutes a first plate of the capacitive element 20, while a second surface 26 of the plate located opposite to the first surface 25 is secured on a conducting surface 31, which is formed on the first surface 13 of the insulating substrate 14. The conducting surface 31 adjoins the metallized holes 21 and 22 so that the electrical continuity with the ground plane 16 is guaranteed. As is appar ent from Figure 1, the conducting surface 31 constitutes a second plate of the capacitive element 20. A recess 32 is provided in the conducting surface 31 opposite to the semiconductor circuit element 12 in order to reduce the capacitance of the conductors.

Figure 2 is a plan view of the plate 24 and shows the arrangement of the conducting "bumps" 27, 28a, 28b, 29a, 29b and of the metallized surfaces 30a and 30b. As is shown in Figure 2, the "bump" 27 is prolonged into a metallized track 37, while the "bumps" 28a, 28b are connected to another metal track 38. The drain zone and the gate of the field effect transistor 12 can be connected through these tracks 37 and 38, respectively, to other circuit elements by means of the wires 47 and 48.

Figure 3 is a partial sectional view of the intermediate element 23, which figure shows an embodiment of the metallized surfaces 30a and 30b and of the conducting "bumps" 29a and 29b; only these are represented for the sake of clarity. The plate 24 has first formed on it by photo-etching the surfaces 30a and 30b as well as the tracks 47, 48 after deposition of a first layer 41a, 41b, obtained by cathode sputtering of nickel, chromium and gold and after the subsequent formation of a second layer 42a, 42b of gold deposited electrolytically. During a second photo-etching step, the "bumps" 29a and 29b are formed after the successive electrodeposition of protuberances 43a, 43b of copper and of tin-iodine solder layers 44a, 44b.

Figure 4 shows the circuit diagram of an embodiment of the high-frequency circuit 11 according to the invention for adjusting the field effect transistor 12. In this embodiment, the source zone S of the transistor is connected to the ground plane 16 for the high frequencies through the capacitive element 20, which then must have a high capacitance. For this reason it is favourable that the dielectric material of the intermediate wiring board has a high dielectric constant between 600 and 2000. Among the materials that can be used are glass, ceramic material and barium titanate. A polarization resistor R5 can thus be arranged parallel to the capacitive element 20 so that in co-operation with the stabilization circuit 50 a working point for current and for voltage can be defined which is independent of the field effect transistor.

In the presence of the bipolar transistor T, the stabilization circuit 50 in fact keeps the current I_D through the field effect transistor 12 substantially constant. Since the drain zone potential is fixed, the potential difference V_{DS} between the drain zone and the source zone consequently is also substantially constant. The working point for current I_D and for voltage V_{DS} of the field effect transistor is therefore adjusted independently of the dispersion existing between the transistor of the same kind and more particularly of the sometimes large dispersion of the potential difference V_{GS} between the gate G and the source zone S. By way of example, the numerical values of the main parameters of the circuit of Figure 4 are as follows.

V = 8V
R1 = 2700 Ω
R2 = 6200Ω
R = 180 Ω
R4 = 2200 Ω
R5 = 330 Ω

The invention is not limited to the embodiment of a field effect transistor shown in Figure 1 and 2. As a matter of course, the invention may also be realized by means of other circuit elements, such as bipolar transistors or diodes.

CLAIMS

1. A high-frequency circuit comprising at least a semiconductor circuit element which is arranged on the side of a first surface of an insulating substrate, a second surface of this substrate located opposite to the first surface being at least partly metallized in order to form a ground plane, while the semiconductor element is provided with electrodes each having at least an output terminal, one of the electrodes, which is referred to as first electrode, being intended to be electrically connected to the ground plane through a capacitive element and an electrical connection with the ground plane being established by means of a metallized hole through the insulating substrate, characterized in that the semiconductor circuit element is secured on an intermediate connection element provided with a plate of a dielectric material having protruding parts of a conducting material which are present on a first surface and on

which the output terminals of the electrodes of the semiconductor circuit element are directly soldered, each protruding part, which is connected to output terminals of the first electrode, being conductively connected to a conducting surface which is formed on the first surface of the plate and constitutes a first plate of the capacitive element, while a second surface of the plate, which is located opposite to the first surface, is secured on at least one first surface of the insulating substrate formed on the conducting surface which contacts at least one metallized hole and constitutes the second plate of the capacitive element.

2. A high-frequency circuit as claimed in Claim 1, characterized in that the semiconductor circuit element is a field effect transistor and in that the said first electrode contacts the source zone of the field effect transistor.

3. A high-frequency circuit as claimed in anyone of Claims 1 or 2, characterized in that the dielectric material constituting the plate of the intermediate wiring board has a dielectric constant between 600 and 2000.

4. A high-frequency circuit as claimed in anyone of Claims 1 to 3, characterized in that a recess is provided in the conducting surface opposite to the semi-conductor circuit element.

5. A high-frequency circuit as claimed in Claim 2, characterized in that the source zone of the field effect transistor is capacitively connected for high frequencies to the ground plane and in that a resistor of fixed value arranged parallel to the capacitive element connects the source zone for low frequencies to the ground plane, while through a stabilization circuit the current and the voltage of the field effect transistor are adjusted so that the working point is independent of the field effect transistor.

6. A high-frequency circuit substantially as herein described with reference to Figures 1 to 3 or Figure 4 of the accompanying drawings.

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